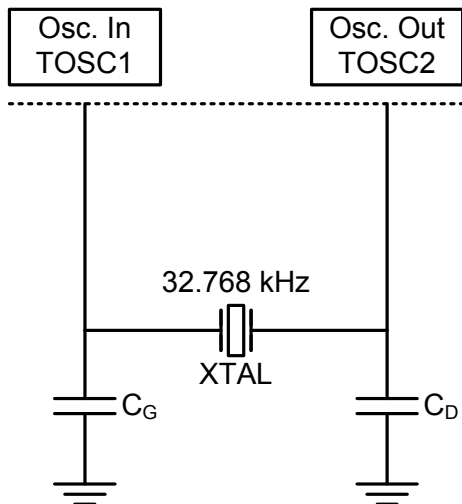


Pierce Oscillator

Design and Crystal
Recommendations

Atmel
ATxmega "Normal Mode"

ATxmegaA1/A3/A4/D3/D4



Oscillator Design Check

Test Conditions			
Power Supply Voltage V_{DD}	1.7	3.6	V
Load Capacitors C_D / C_G	12 / 12		pF
Results			
Effective Load Capacitance	9.2	8.9	pF
Oscillation Allowance	410	435	k Ω
Oscillator Output Voltage AC	280	280	mV _{RMS}
Drive Level	0.075	0.070	μ W
Startup Time	500	500	ms
Overtone Mode Suppression	Safe		----

Recommendation

Crystal		
Crystal Type	MS3V-T1R / CC7V-T1A	
Frequency	32.768	kHz
Load Capacitance C_L	9.0	pF
Tolerance	+/-20	ppm
Oscillator Design		
C_D	12	pF
C_G	12	pF

Remarks

The ATmegaA1/A3/A4/D3/D4 consists of a self limiting Pierce Oscillator.

Using "Normal Mode" results in the following oscillator's characteristics:

Placing $C_D = 12$ pF and $C_G = 12$ pF load capacitors on each side of the crystal results in an effective load capacitance of 9.2 pF at $V_{DD} = 1.7$ V and 8.9 pF at $V_{DD} = 3.6$ V (including board stray capacitances) which are perfect matches for a crystal specified for $C_L = 9.0$ pF.

The oscillator circuit provides an oscillation allowance of 410 k Ω at $V_{DD} = 1.7$ V and 435 k Ω at $V_{DD} = 3.6$ V; this allows the safe use of small SMD quartz crystals ($ESR \leq 80$ k Ω).

Date: November 2010

Revision N°: 1.0

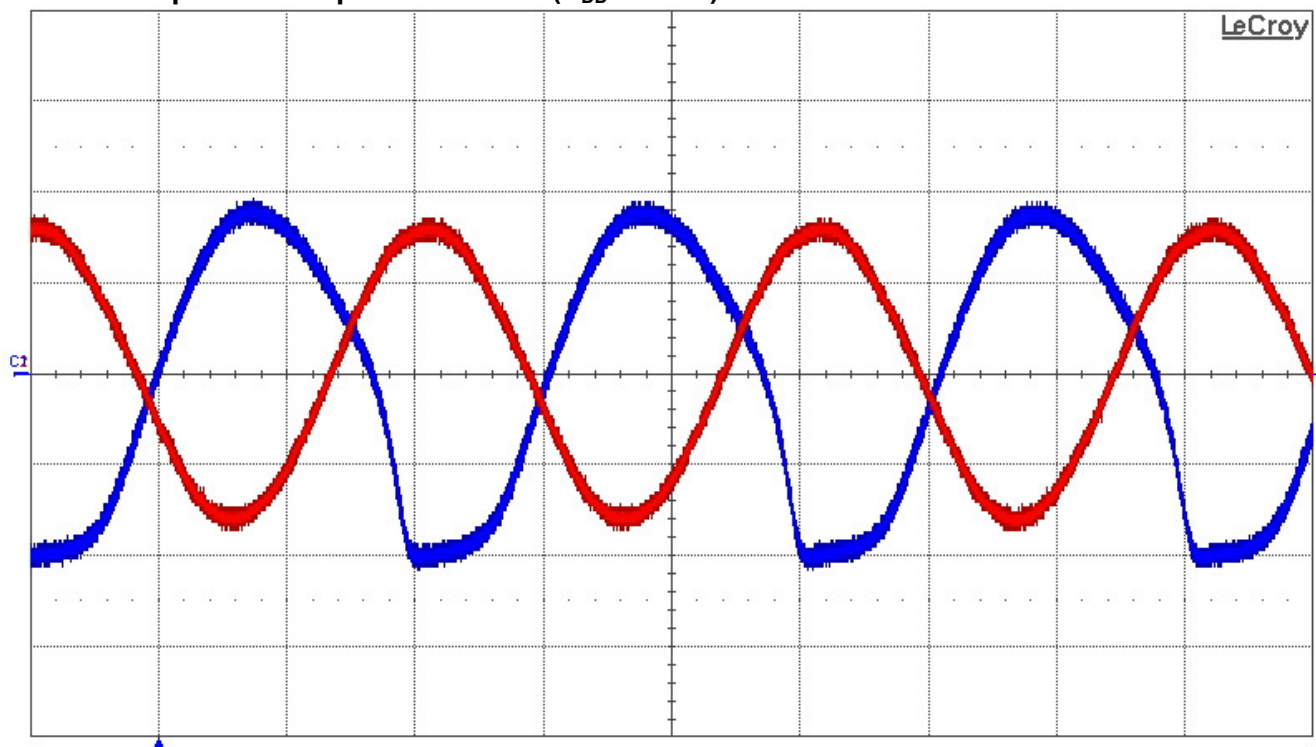
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In accordance with our policy of continuous development and improvement,
Micro Crystal reserves the right to modify specifications or design-recommendations without prior notice.
The recommendations stated above are based on measured-results, respecting the "oscillator design rules".
Micro Crystal makes no representation or warranty for information in this "Design and Crystal Recommendations".

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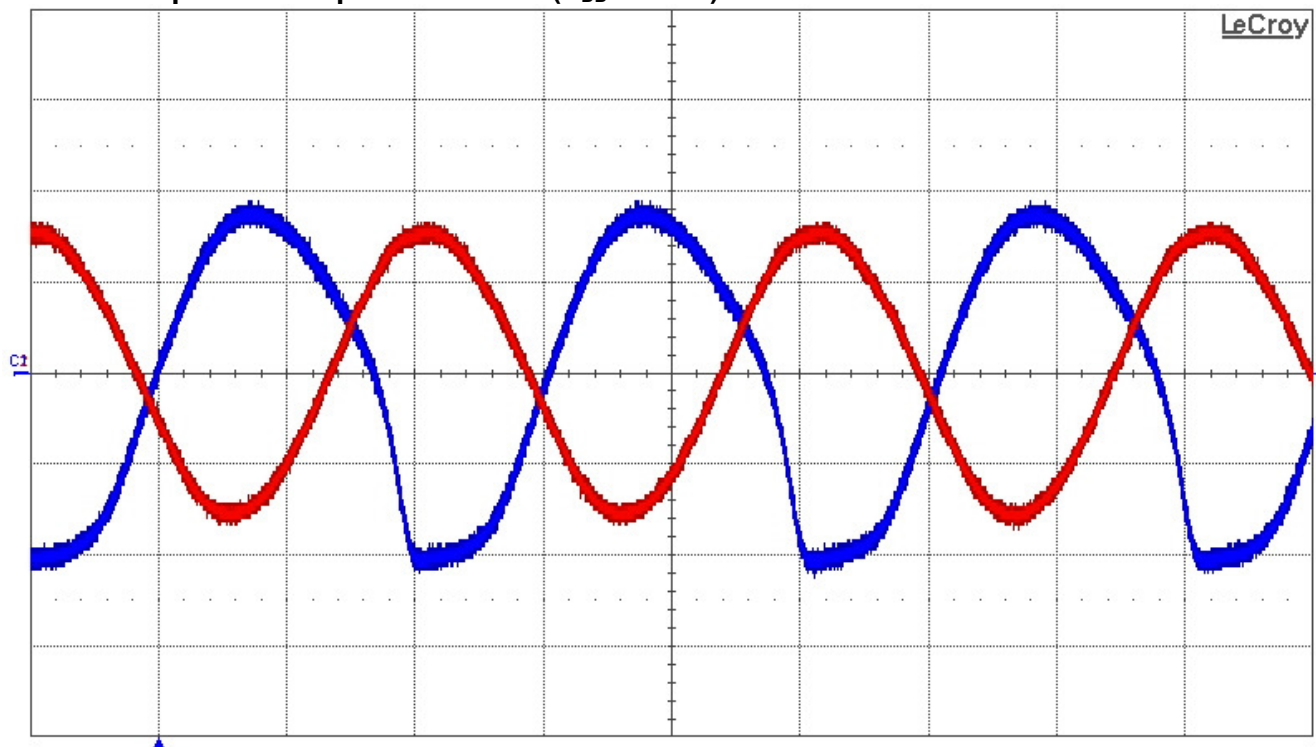
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Oscillator Input and Output waveforms ($V_{DD} = 1.7\text{ V}$):



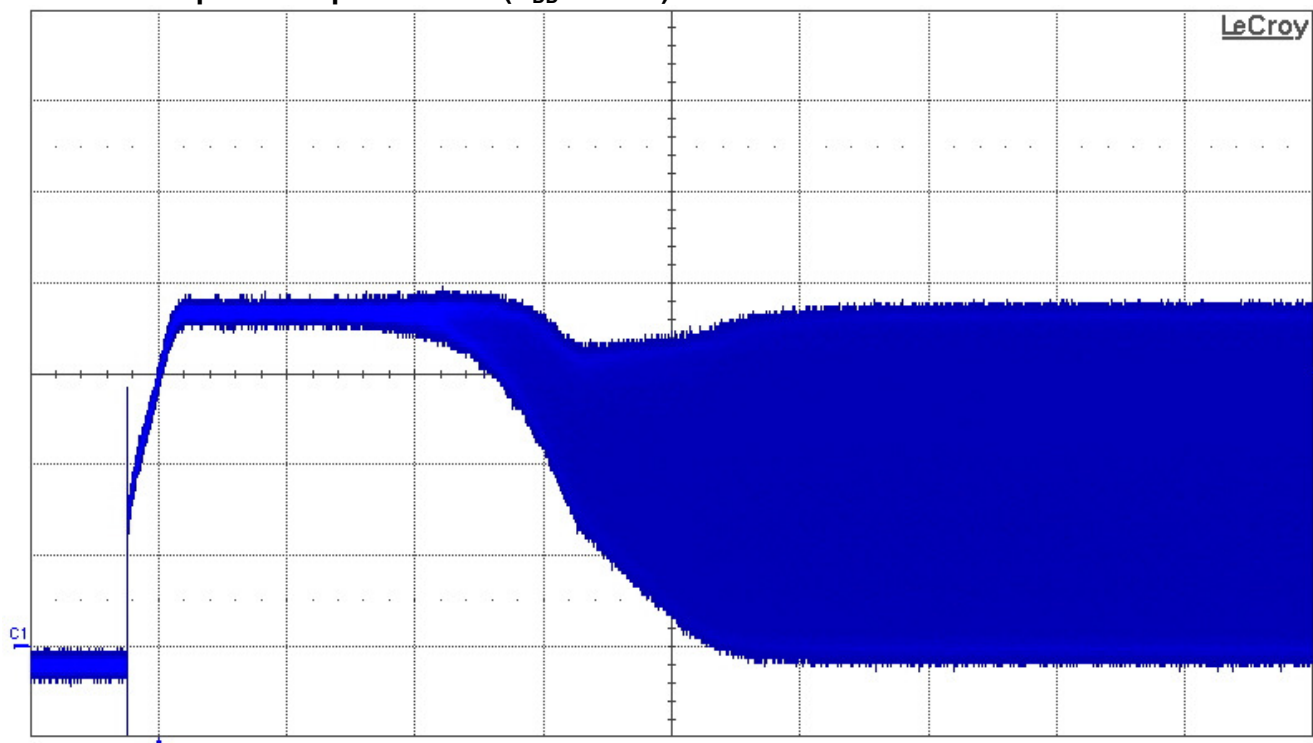
■ C1: Osc. Out (200 mV/div - AC) ■ C2: Osc. In (200 mV/div - AC) Time base: 10 $\mu\text{s}/\text{div}$

Oscillator Input and Output waveforms ($V_{DD} = 3.6\text{ V}$):



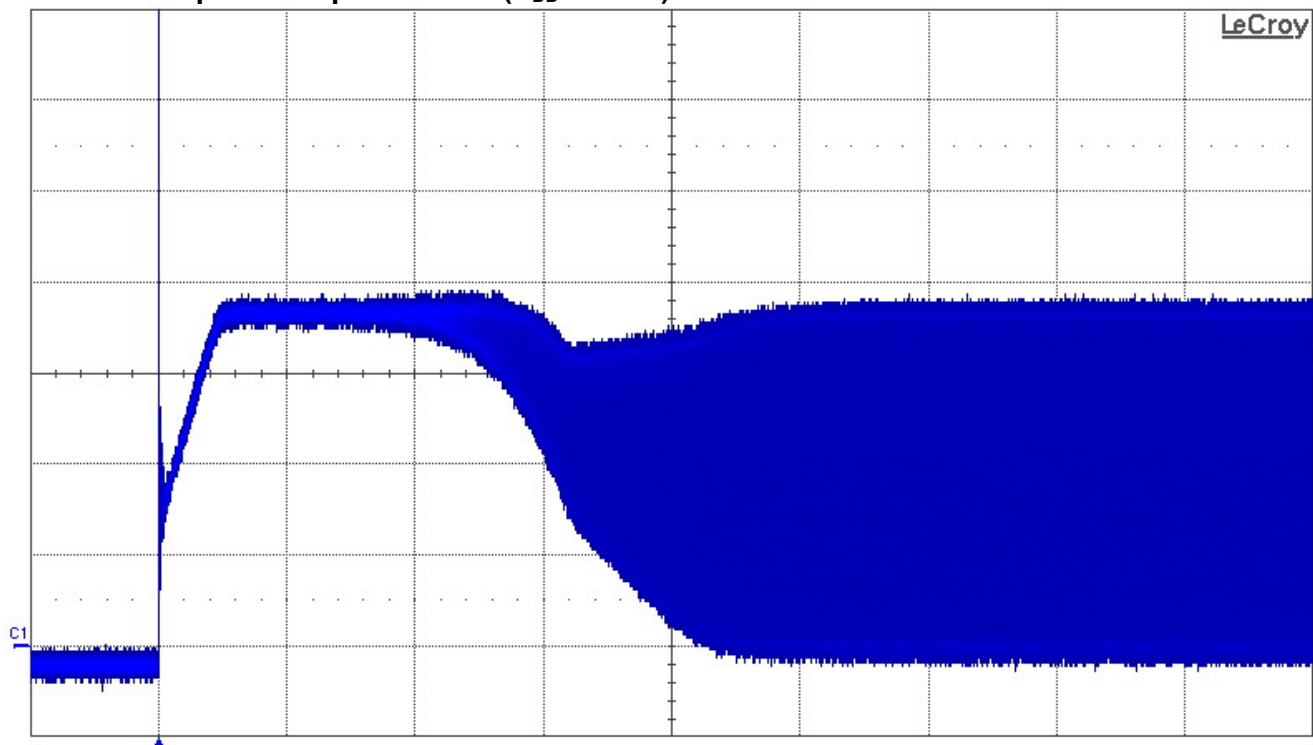
■ C1: Osc. Out (200 mV/div - AC) ■ C2: Osc. In (200 mV/div - AC) Time base: 10 $\mu\text{s}/\text{div}$

Oscillator Output startup waveform ($V_{DD} = 1.7\text{ V}$):



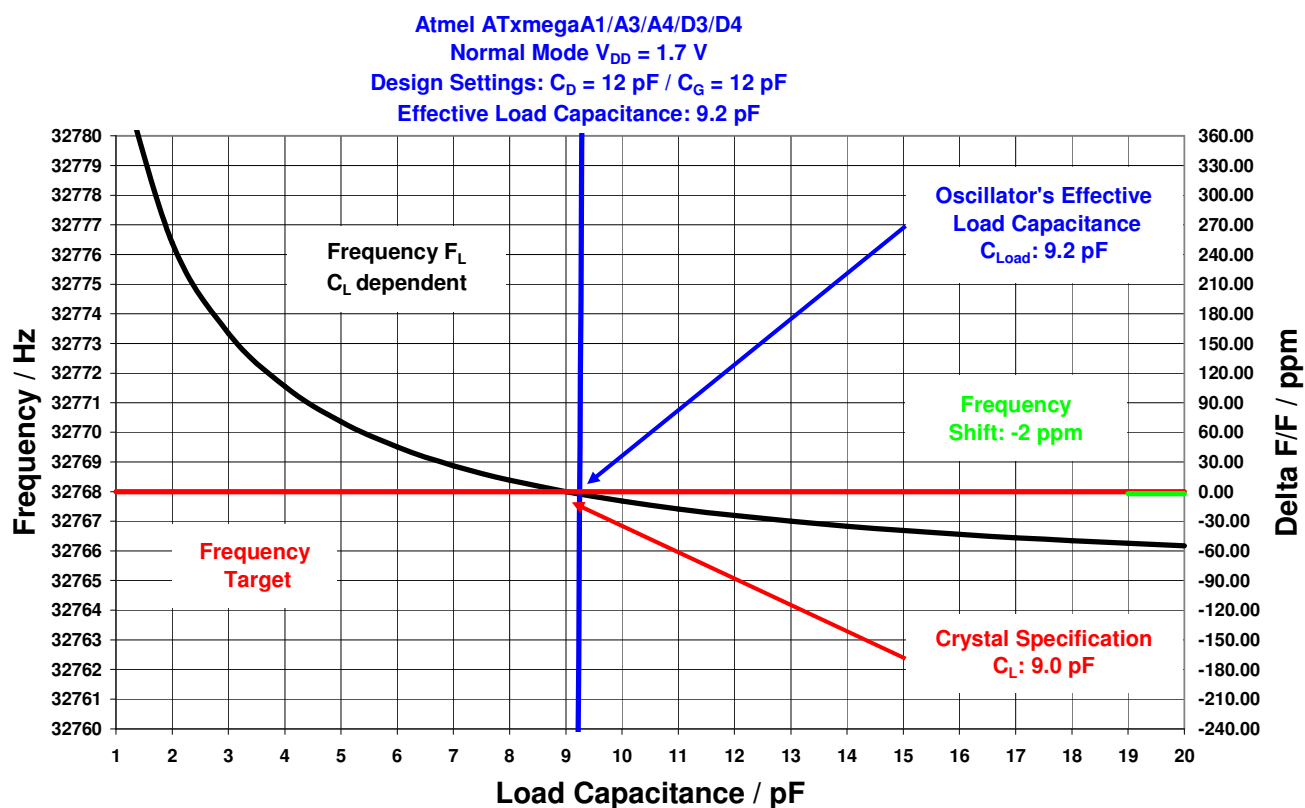
■ C1: Osc. Out (200 mV/div - DC) Time base: 100 ms/div

Oscillator Output startup waveform ($V_{DD} = 3.6\text{ V}$):



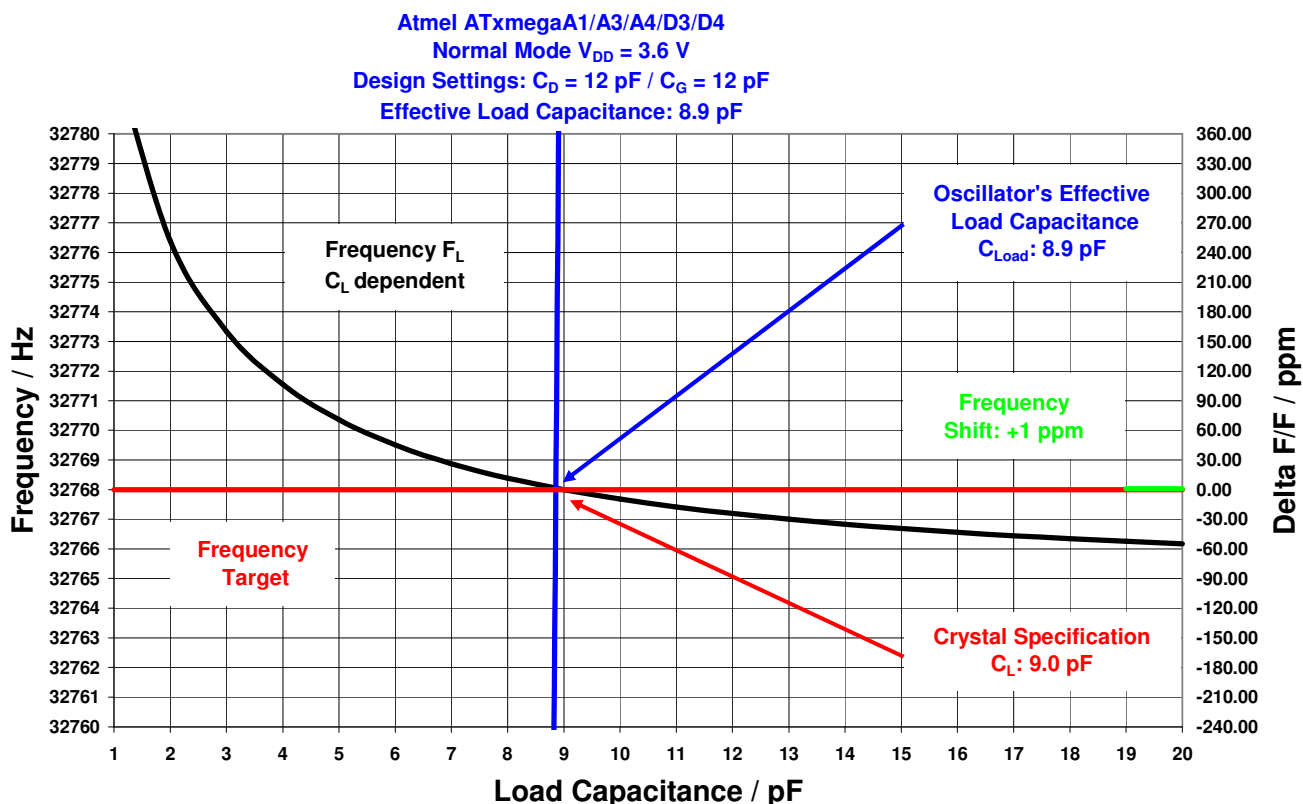
■ C1: Osc. Out (200 mV/div - DC) Time base: 100 ms/div

Crystal matching chart ($V_{DD} = 1.7\text{ V}$):



As shown in the chart above, an effective load capacitance of 9.2 pF results in a frequency offset of -2 ppm using a MS3V-T1R crystal specified for $C_L = 9.0\text{ pF}$.

Crystal matching chart ($V_{DD} = 3.6$ V):



As shown in the chart above, an effective load capacitance of 8.9 pF results in a frequency offset of +1 ppm using a MS3V-T1R crystal specified for $C_L: 9.0$ pF.

Remarks:

On a final product, with optimized PCB layout (smaller crystal's pads and crystal placed close to the IC), the stray capacitances will likely be smaller. Due to that, the effective load capacitance will be reduced. In this case, in order to still achieve a perfect crystal's matching, the external load capacitors value (C_D and C_G) has to be increased.